Fig. 1

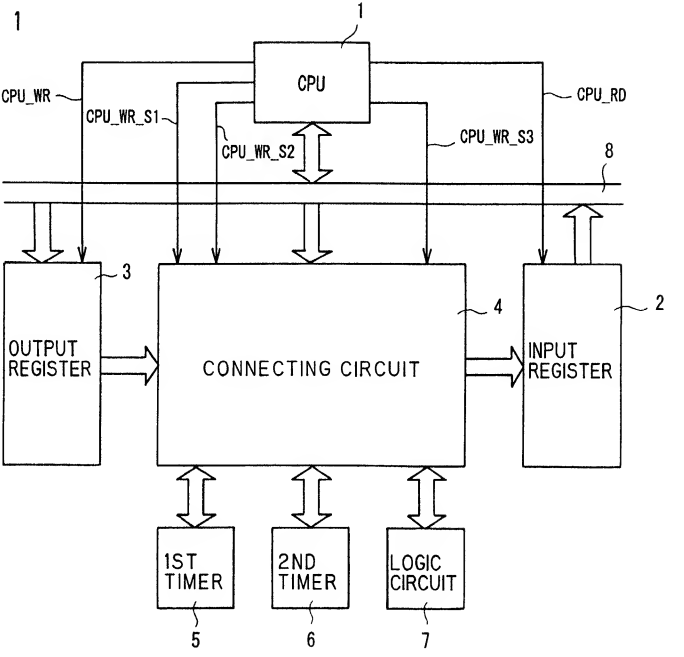

1
CPU
CPU_WR
CPU_WR_S1
CPU_WR_S2
CPU_WR_S3
CPU_RD
8
3
OUTPUT REGISTER
4
CONNECTING CIRCUIT
2
INPUT REGISTER
1ST TIMER
2ND TIMER
LOGIC CIRCUIT
5
6
7

Fig. 2

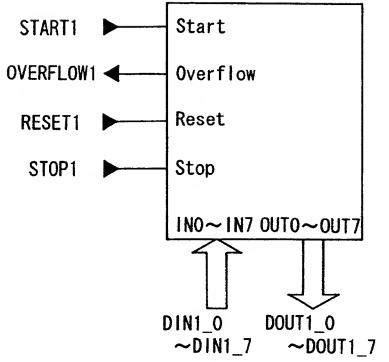

START1
Start
OVERFLOW1
Overflow
RESET1
Reset
STOP1
Stop
IN0～IN7 OUT0～OUT7
DIN1_0
～DIN1_7
DOUT1_0
～DOUT1_7

Fig. 3

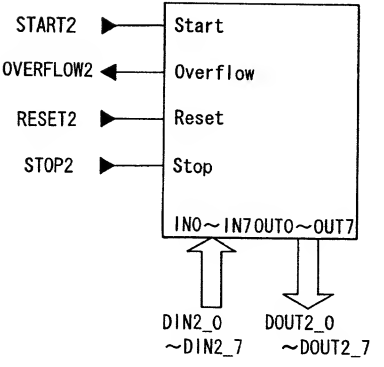
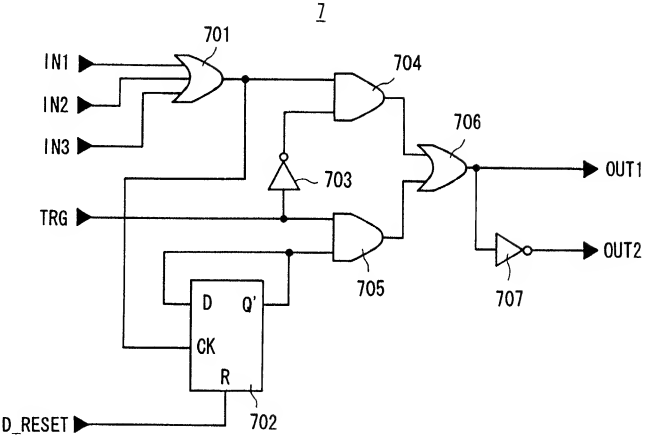

START2
Start
OVERFLOW2
Overflow
RESET2
Reset
STOP2
Stop
IN0～IN7 OUT0～OUT7
DIN2_0
～DIN2_7
DOUT2_0
～DOUT2_7

Fig. 4


7
701
IN1
IN2
IN3
704
706
703
OUT1
TRG
OUT2
705
707
D
Q'
CK
R
D_RESET
702

T0012-020120001

Fig. 5

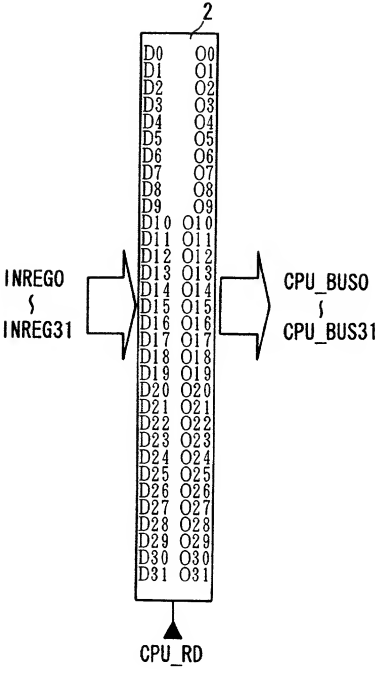


Fig. 6

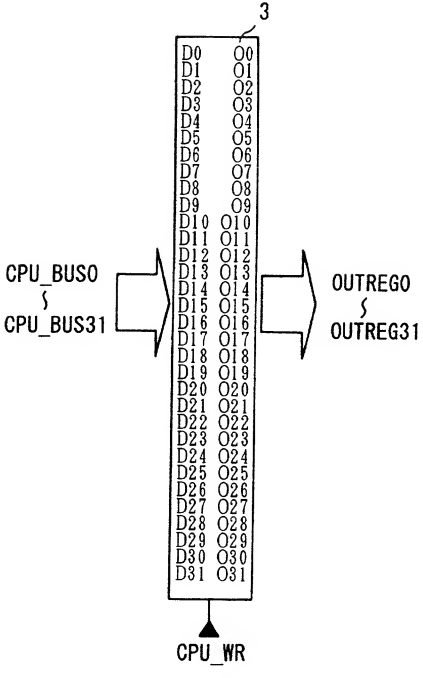

3
D0 O0
D1 O1
D2 O2
D3 O3
D4 O4
D5 O5
D6 O6
D7 O7
D8 O8
D9 O9
D10 O10
D11 O11
D12 O12
D13 O13
D14 O14
D15 O15
D16 O16
D17 O17
D18 O18
D19 O19
D20 O20
D21 O21
D22 O22
D23 O23
D24 O24
D25 O25
D26 O26
D27 O27
D28 O28
D29 O29
D30 O30
D31 O31
CPU_BUS0
~
CPU_BUS31
OUTREG0
~
OUTREG31
CPU_WR

Fig. 7

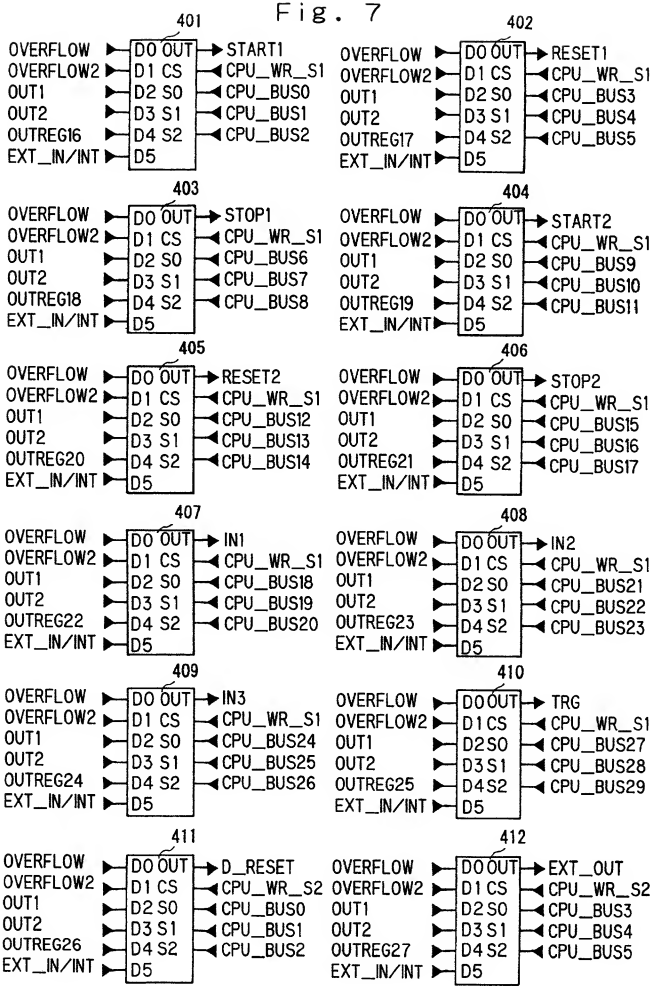



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Fig. 8

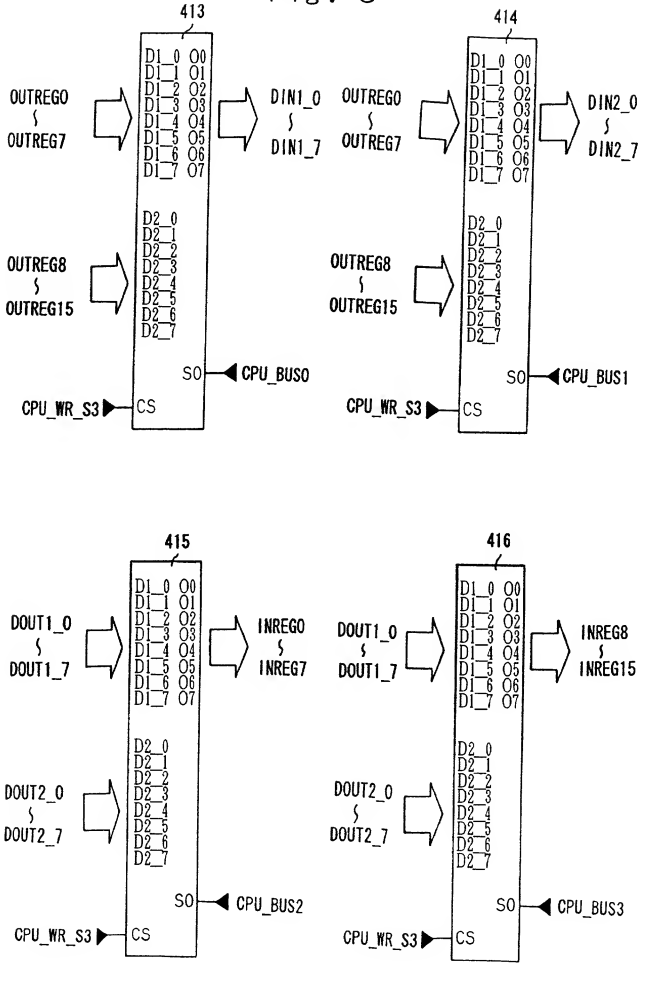


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Fig. 9

| S2 | S1 | S0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | D0 |
| 0 | 0 | 1 | D1 |
| 0 | 1 | 0 | D2 |
| 0 | 1 | 1 | D3 |
| 1 | 0 | 0 | D4 |
| 1 | 0 | 1 | D5 |
| 1 | 1 | 0 | — |
| 1 | 1 | 1 | — |

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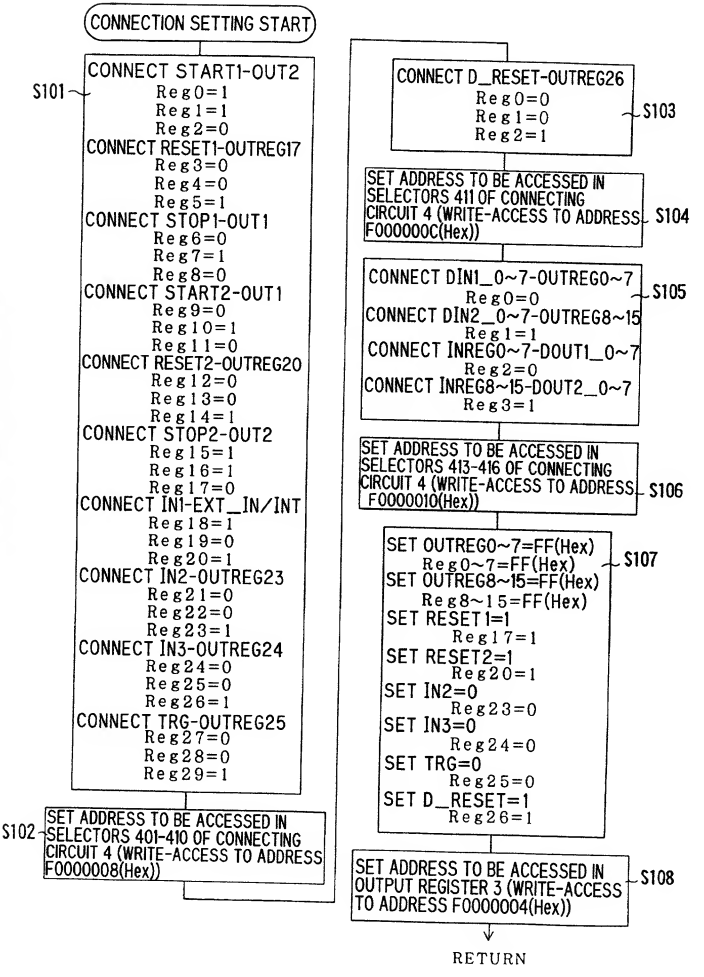
Fig. 10




FOOTER 02CT2007

Fig. 11

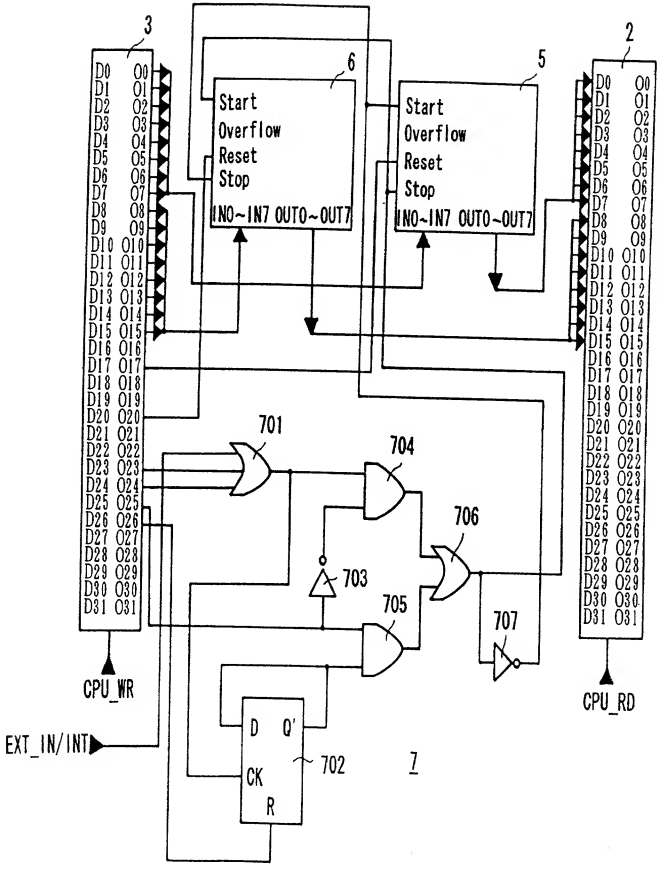

3
2
6
5
Start
Overflow
Reset
Stop
IN0~IN7 OUT0~OUT7
D0 O0
D1 O1
D2 O2
D3 O3
D4 O4
D5 O5
D6 O6
D7 O7
D8 O8
D9 O9
D10 O10
D11 O11
D12 O12
D13 O13
D14 O14
D15 O15
D16 O16
D17 O17
D18 O18
D19 O19
D20 O20
D21 O21
D22 O22
D23 O23
D24 O24
D25 O25
D26 O26
D27 O27
D28 O28
D29 O29
D30 O30
D31 O31
701
704
706
703
705
707
CPU_WR
CPU_RD
EXT_IN/INT
D Q'
CK
R
702
7

Fig. 12

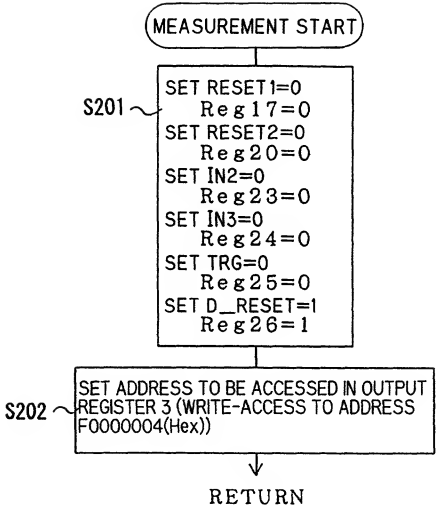

MEASUREMENT START
S201
SET RESET1=0
Reg17=0
SET RESET2=0
Reg20=0
SET IN2=0
Reg23=0
SET IN3=0
Reg24=0
SET TRG=0
Reg25=0
SET D_RESET=1
Reg26=1
S202
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
RETURN

Fig. 13

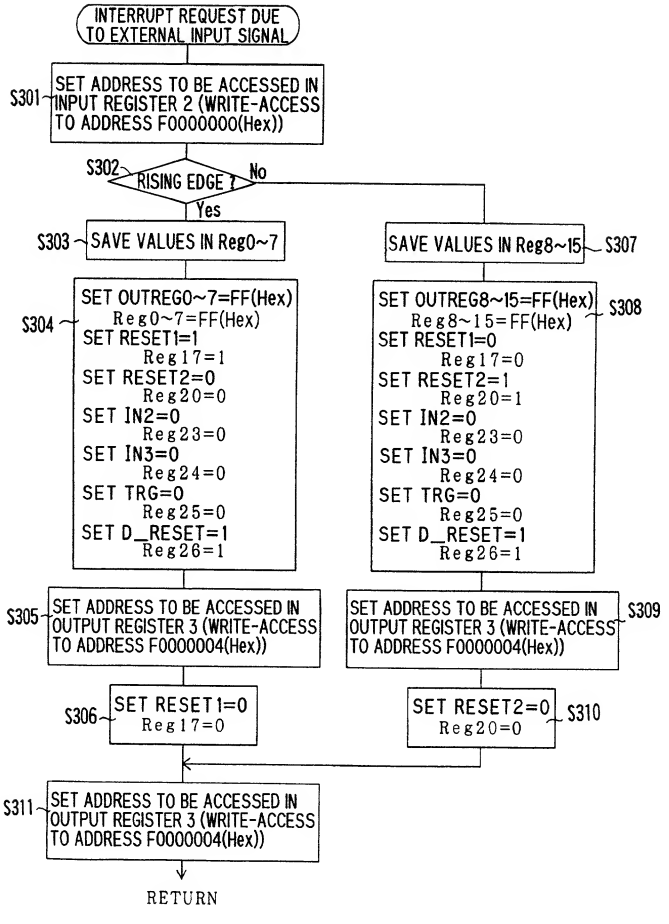

INTERRUPT REQUEST DUE TO EXTERNAL INPUT SIGNAL
S301
SET ADDRESS TO BE ACCESSED IN INPUT REGISTER 2 (WRITE-ACCESS TO ADDRESS F0000000(Hex))
S302
RISING EDGE ?
No
Yes
S303
SAVE VALUES IN Reg0~7
S304
SET OUTREG0~7=FF(Hex)
Reg0~7=FF(Hex)
SET RESET1=1
Reg17=1
SET RESET2=0
Reg20=0
SET IN2=0
Reg23=0
SET IN3=0
Reg24=0
SET TRG=0
Reg25=0
SET D_RESET=1
Reg26=1
S305
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S306
SET RESET1=0
Reg17=0
SAVE VALUES IN Reg8~15
S307
SET OUTREG8~15=FF(Hex)
Reg8~15=FF(Hex)
SET RESET1=0
Reg17=0
SET RESET2=1
Reg20=1
SET IN2=0
Reg23=0
SET IN3=0
Reg24=0
SET TRG=0
Reg25=0
SET D_RESET=1
Reg26=1
S308
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S309
SET RESET2=0
Reg20=0
S310
S311
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
RETURN

Fig. 14

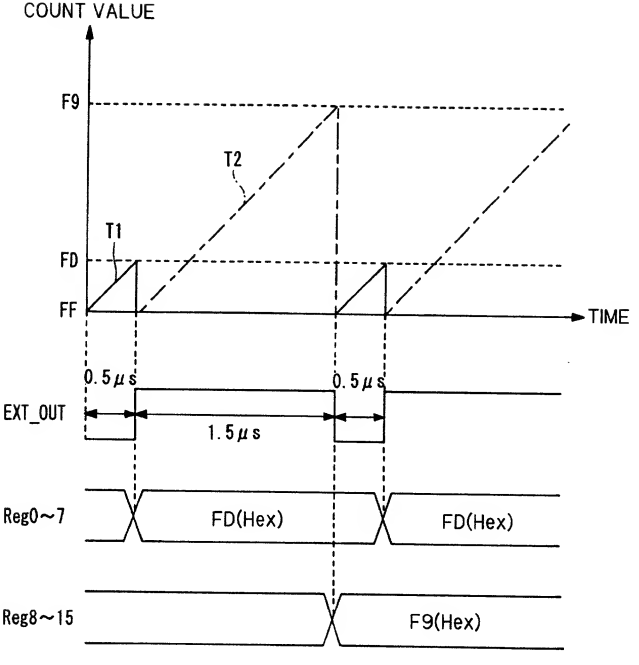

COUNT VALUE
F9
T2
T1
FD
FF
TIME
0.5μs
0.5μs
EXT_OUT
1.5μs
Reg0~7
FD(Hex)
FD(Hex)
Reg8~15
F9(Hex)

Fig. 15

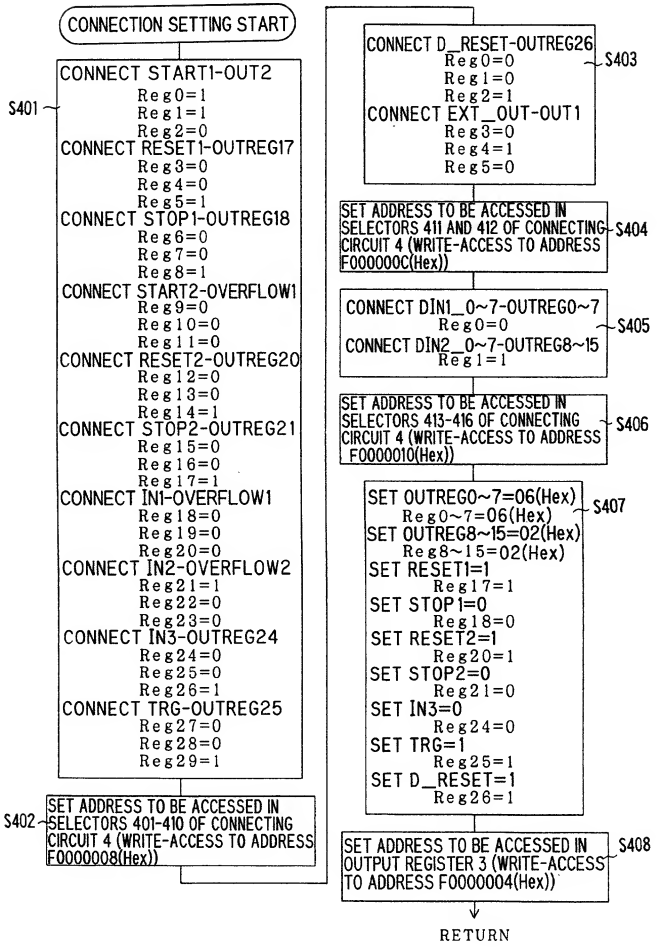

CONNECTION SETTING START
CONNECT START1-OUT2
Reg0=1
Reg1=1
Reg2=0
CONNECT RESET1-OUTREG17
Reg3=0
Reg4=0
Reg5=1
CONNECT STOP1-OUTREG18
Reg6=0
Reg7=0
Reg8=1
CONNECT START2-OVERFLOW1
Reg9=0
Reg10=0
Reg11=0
CONNECT RESET2-OUTREG20
Reg12=0
Reg13=0
Reg14=1
CONNECT STOP2-OUTREG21
Reg15=0
Reg16=0
Reg17=1
CONNECT IN1-OVERFLOW1
Reg18=0
Reg19=0
Reg20=0
CONNECT IN2-OVERFLOW2
Reg21=1
Reg22=0
Reg23=0
CONNECT IN3-OUTREG24
Reg24=0
Reg25=0
Reg26=1
CONNECT TRG-OUTREG25
Reg27=0
Reg28=0
Reg29=1
S401
SET ADDRESS TO BE ACCESSED IN SELECTORS 401-410 OF CONNECTING CIRCUIT 4 (WRITE-ACCESS TO ADDRESS F0000008(Hex))
S402
CONNECT D_RESET-OUTREG26
Reg0=0
Reg1=0
Reg2=1
CONNECT EXT_OUT-OUT1
Reg3=0
Reg4=1
Reg5=0
S403
SET ADDRESS TO BE ACCESSED IN SELECTORS 411 AND 412 OF CONNECTING CIRCUIT 4 (WRITE-ACCESS TO ADDRESS F000000C(Hex))
S404
CONNECT DIN1_0~7-OUTREG0~7
Reg0=0
CONNECT DIN2_0~7-OUTREG8~15
Reg1=1
S405
SET ADDRESS TO BE ACCESSED IN SELECTORS 413-416 OF CONNECTING CIRCUIT 4 (WRITE-ACCESS TO ADDRESS F0000010(Hex))
S406
SET OUTREG0~7=06(Hex)
Reg0~7=06(Hex)
SET OUTREG8~15=02(Hex)
Reg8~15=02(Hex)
SET RESET1=1
Reg17=1
SET STOP1=0
Reg18=0
SET RESET2=1
Reg20=1
SET STOP2=0
Reg21=0
SET IN3=0
Reg24=0
SET TRG=1
Reg25=1
SET D_RESET=1
Reg26=1
S407
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S408
RETURN

Fig. 16

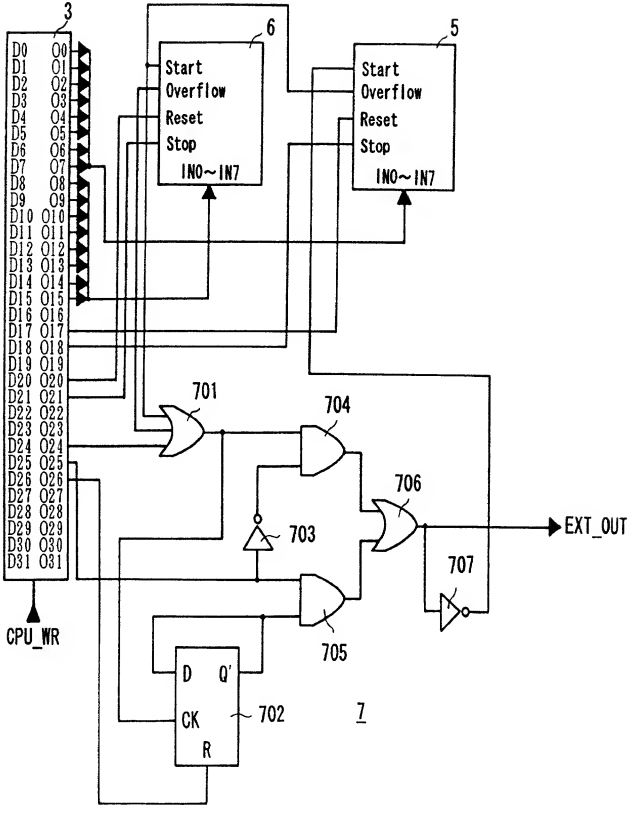

3
6
5
Start
Overflow
Reset
Stop
IN0~IN7
D0 O0
D1 O1
D2 O2
D3 O3
D4 O4
D5 O5
D6 O6
D7 O7
D8 O8
D9 O9
D10 O10
D11 O11
D12 O12
D13 O13
D14 O14
D15 O15
D16 O16
D17 O17
D18 O18
D19 O19
D20 O20
D21 O21
D22 O22
D23 O23
D24 O24
D25 O25
D26 O26
D27 O27
D28 O28
D29 O29
D30 O30
D31 O31
CPU_WR
701
704
706
703
707
705
EXT_OUT
D
Q'
CK
R
702
7

Fig. 17

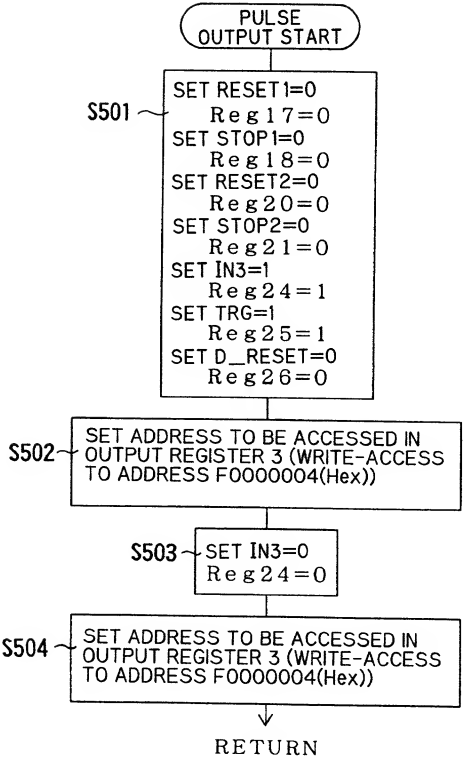

PULSE OUTPUT START
S501
SET RESET1=0
Reg17=0
SET STOP1=0
Reg18=0
SET RESET2=0
Reg20=0
SET STOP2=0
Reg21=0
SET IN3=1
Reg24=1
SET TRG=1
Reg25=1
SET D_RESET=0
Reg26=0
S502
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S503
SET IN3=0
Reg24=0
S504
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
RETURN

Fig. 18

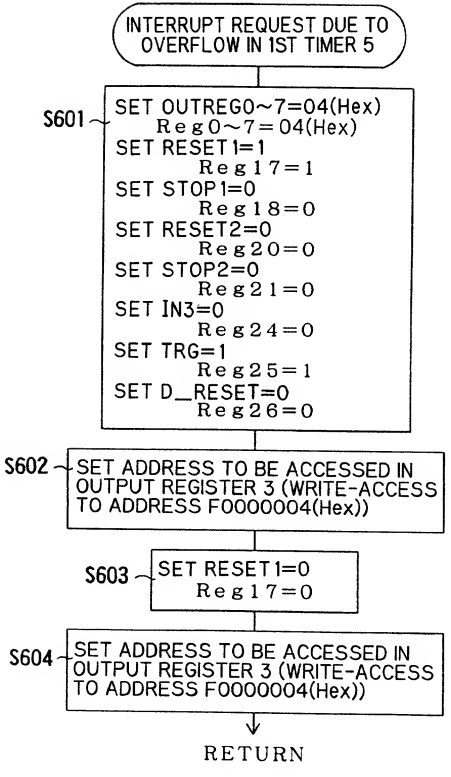

INTERRUPT REQUEST DUE TO OVERFLOW IN 1ST TIMER 5
S601
SET OUTREG0~7=04(Hex)
Reg0~7=04(Hex)
SET RESET1=1
Reg17=1
SET STOP1=0
Reg18=0
SET RESET2=0
Reg20=0
SET STOP2=0
Reg21=0
SET IN3=0
Reg24=0
SET TRG=1
Reg25=1
SET D_RESET=0
Reg26=0
S602
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S603
SET RESET1=0
Reg17=0
S604
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
RETURN

Fig. 19

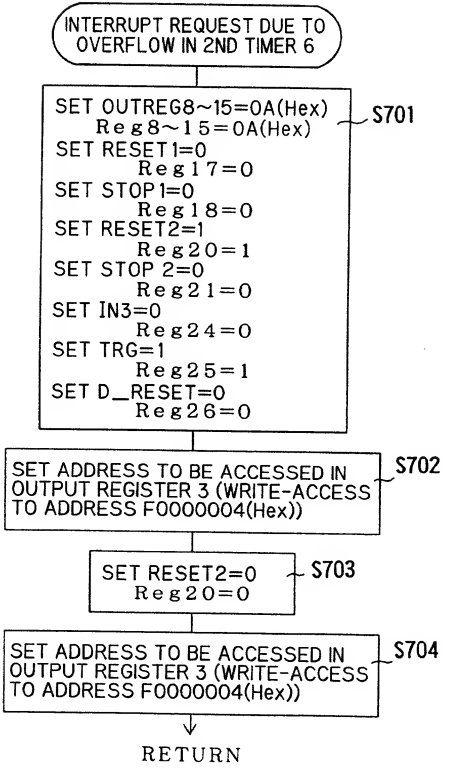

INTERRUPT REQUEST DUE TO OVERFLOW IN 2ND TIMER 6
SET OUTREG8~15=0A(Hex)
Reg8~15=0A(Hex)
S701
SET RESET1=0
Reg17=0
SET STOP1=0
Reg18=0
SET RESET2=1
Reg20=1
SET STOP 2=0
Reg21=0
SET IN3=0
Reg24=0
SET TRG=1
Reg25=1
SET D_RESET=0
Reg26=0
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S702
SET RESET2=0
Reg20=0
S703
SET ADDRESS TO BE ACCESSED IN OUTPUT REGISTER 3 (WRITE-ACCESS TO ADDRESS F0000004(Hex))
S704
RETURN

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Fig. 20

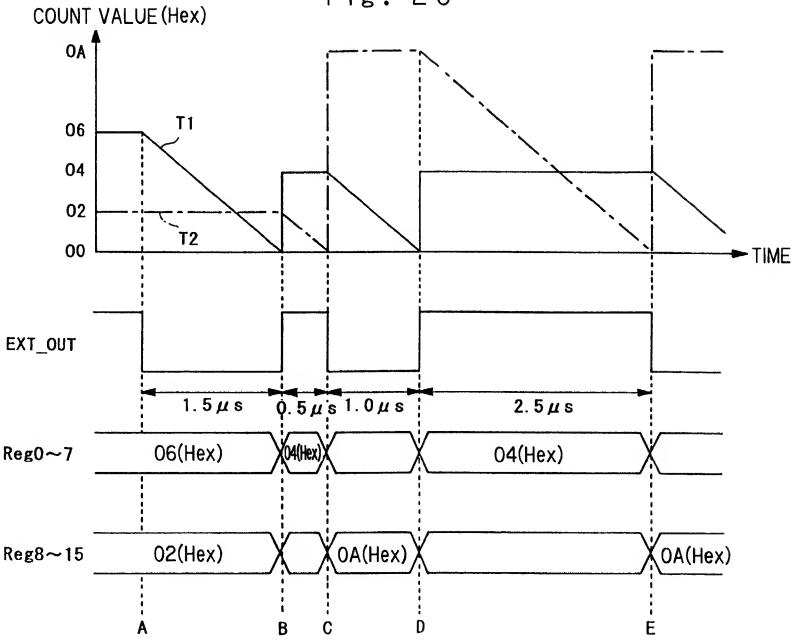


Fig. 21 PRIOR ART

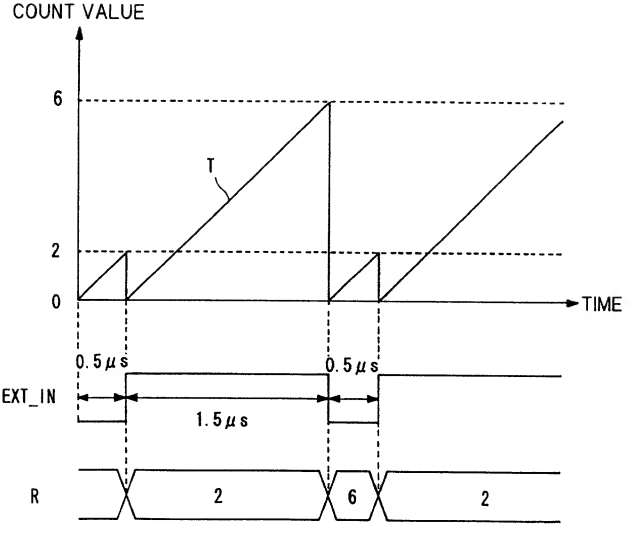


Fig. 22 PRIOR ART

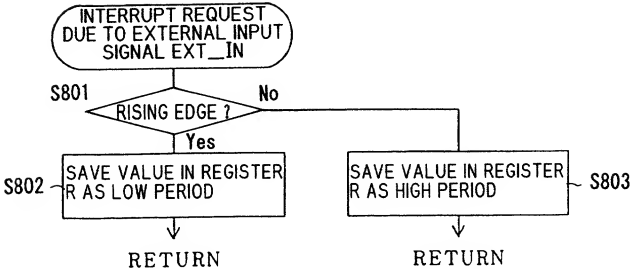


Fig. 23 PRIOR ART

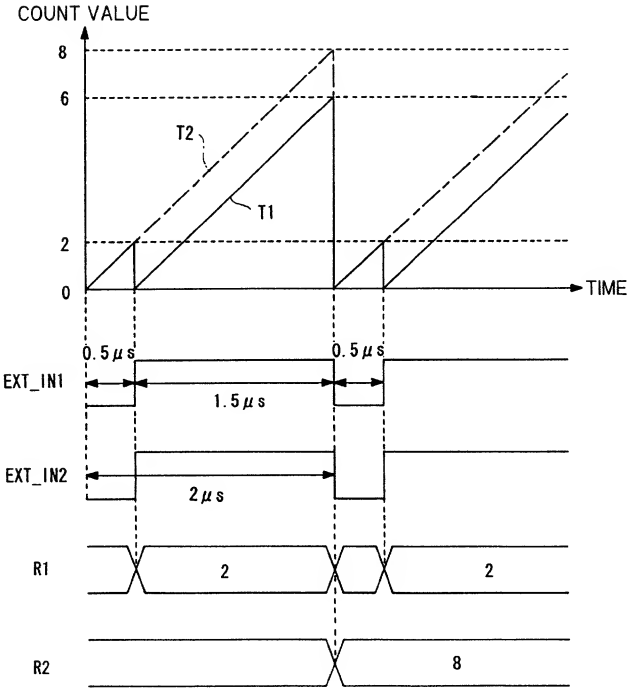
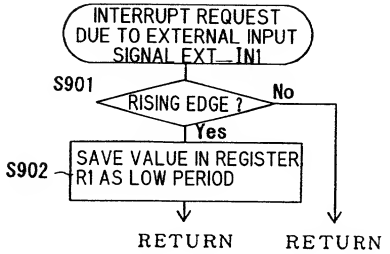


Fig. 24 PRIOR ART



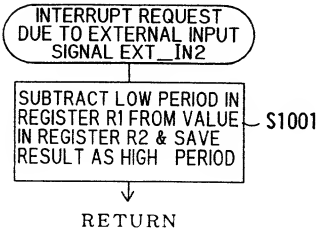


Fig. 25 PRIOR ART